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Active Memory Architecture, Early Design

Wednesday, 3 December 2025 18:45 (15 minutes)

The Active Memory Architecture (AMA) is a non von Neumann, is a memory-centric, non von Neumann, graph processing architecture for scaling to Zettaflops performance with first production delivery in 2031.graph processing computer architecture for scaling to Zettaflops performance capability. Its first commercial production delivery is scheduled for 2031. The AMA project is in its second year of design at the Texas Advanced Computing Center. AMA is a product of more than three decades of exploratory research in parallel computing including parallel execution models, dynamic runtime systems, hardware architecture, and parallel programming. Strictly speaking, it is not conventional with respect to typical von Neumann processor cores. The memory and logic are merged with small chunks of data (about 1 K wide words) and logic in message-driven units called “Fontons”. The messages are “Operons” that carry both data and work to any Fonton in the global system. The name space combines attributes of both virtual and physical addressing across the system. The distribution of work is dynamic and changes during the computation for optimal operation. This closing short presentation of CHPC25 will update the international HPC community on this revolutionary method immediately following the presentation of Dr. Dan Stanzione, Director of TACC.

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