



Contribution ID: 49

Type: **Talk**

KEYNOTE 7: Coreless Continuum Computer Architecture

Wednesday, 5 December 2018 18:00 (45 minutes)

Coreless Continuum Computer Architecture

Thomas Sterling (Department of Intelligent Systems Engineering, School of Informatics, Computing, and Engineering, Indiana University)

As introduced at CHPC-17, a new era is dawning: the Neo-Digital Age as semiconductor fabrication enters its final phase with nano-scale feature size. For the first time in three decades, fundamental technology limitations of device density, power consumption, clock rate, and instruction level parallelism are demanding revolutionary practices to further expand HPC capabilities into the trans-exascale performance regime and perhaps beyond. Among the domains of possible change are those uncovered in the prevailing assumptions embodied by the many generations exploiting Moore's Law, which no longer apply. These include 1) the use of static methods for parallel application programming and static resource management, and 2) the implicit underlying principles buried in the von Neumann architecture of which essentially all HPC systems are since derivatives. An alternative strategy, bordering on a paradigm shift, reverses conventional methodologies a) to employ dynamic adaptive methods of resource management and task scheduling, and b) to eliminate von Neumann bottlenecks, eliminating even the basic core that has endured as the foundation of HPC architecture design since the late 1940s. Central to the forward looking revolution is the elimination of the FPU/ALU as the precious resource with the implied objective function of highest possible utilization. The Continuum Computer Architecture (CCA) has been proposed as a family of alternative architectures that address the current challenge and exploit the future opportunities by fully integration of logic, memory, control, and communication within a single highly replicated computing cell. First suggested an abstract in last year's last Keynote, this presentation will expose key details in structure and semantics that will layout the conceptual scaffolding for future development and application such as machine learning and intelligence, planning, scheduling, hypothesis testing, facial recognition and many other graph-based application. Questions will be encouraged by participants throughout the presentation as well as the Q&A session at the end.

Presenter Biography

Primary author: STERLING, Thomas (Indiana University)

Presenter: STERLING, Thomas (Indiana University)

Session Classification: KEYNOTE 6: Thomas Sterling, Indiana University

Track Classification: HPC Techniques and Computer Science